

CLAIMS

- 1. A computer system comprising:
- a first block which includes multiple processing subsystem means;
- a second block which includes multiple processing subsystem means;
- a third block which includes multiple processing subsystem means;
- a fourth block which includes multiple processing subsystem means;
- a first communication and processing subsystem means that interconnects subsystem means of the first and second blocks;
- a second communication and processing subsystem means that interconnects subsystem means of the third and fourth blocks;
- a third communication and processing subsystem means that interconnects subsystem means of the first and fourth blocks; and
- a fourth communication and processing subsystem means that interconnects subsystem means of the second and third blocks;

wherein respective subsystem means include a respective processing elements and a respective communication and processing unit interconnecting the respective processing elements.

2. A computer system comprising:

first, second, third and fourth blocks of processing subsystems in which each subsystem includes a respective first processing unit and a respective second processing unit and a respective communication and processing unit interconnecting the respective first and second units;

wherein respective first processing unit includes multiple respective processing elements that are networked together;

wherein respective second processing unit includes multiple respective processing elements that are networked together;

wherein corresponding processing elements of respective first processing units of the **first block** are interconnected with each other;

wherein corresponding processing elements of respective second processing units of the **first block** are interconnected with each other;

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wherein corresponding processing elements of respective first processing units of the **second block** are interconnected with each other;

wherein corresponding processing elements of respective second processing units of the **second block** are interconnected with each other;

wherein corresponding processing elements of respective first processing units of the **third** block are interconnected with each other;

wherein corresponding processing elements of respective second processing units of the **third block** are interconnected with each other;

wherein corresponding processing elements of respective fourth processing units of the **fourth block** are interconnected with each other;

wherein corresponding processing elements of respective second processing units of the **fourth block** are interconnected with each other;

a first communication and processing subsystem in which respective processing elements of a first processing unit thereof interconnect with respective communication and processing units of respective processing subsystems of the first block and in which respective processing elements of a second processing unit thereof interconnect with respective communication and processing units of respective processing subsystems of the second block;

a second communication and processing subsystem in which respective processing elements of a first processing unit thereof interconnect with respective communication and processing units of respective processing subsystems of the third block and in which respective processing elements of a second processing unit thereof interconnect with respective communication and processing units of respective processing subsystems of the fourth block;

a third communication and processing subsystem in which respective processing elements of a first processing unit thereof interconnect with respective communication and processing units of respective processing subsystems of the first block and in which respective processing elements of a second processing unit thereof interconnect with respective communication and processing units of respective processing subsystems of the fourth block; and

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a fourth communication and processing subsystem in which respective processing elements of a first processing unit thereof interconnect with respective communication and processing units of respective processing subsystems of the second block and in which respective processing elements of a second processing unit thereof interconnect with respective communication and processing units of respective processing subsystems of the third block.

3. A method of interconnecting a multiplicity of processing elements to produce a computer system architecture:

interconnecting a multiplicity of processing elements to produce a plurality of processing subsystems which respectively include a respective first processing units and respective second processing units and respective communication and processing units interconnecting respective first and second processing units;

interconnecting a **first** group of the plurality of processing subsystems to produce a **first** block of subsystems in which respective processing elements of respective first processing units of respective processing subsystems of the **first** block are interconnected with each other and in which respective processing elements of respective second processing units of respective processing subsystems of the first block are interconnected with each other;

interconnecting a **second** group of the plurality of processing subsystems to produce a **second** block of subsystems in which respective processing elements of respective first processing units of respective processing subsystems of the **second** block are interconnected with each other and in which respective processing elements of respective second processing units of respective processing subsystems of the **second** block are interconnected with each other;

interconnecting a **third** group of the plurality of processing subsystems to produce a **third** block of subsystems in which respective processing elements of respective first processing units of respective processing subsystems of the **third** block are interconnected with each other and in which respective processing elements of respective second processing units of respective processing subsystems of the **third** block are interconnected with each other;

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interconnecting a **fourth** group of the plurality of processing subsystems to produce a **fourth** block of subsystems in which respective processing elements of respective first processing units of respective processing subsystems of the **fourth** block are interconnected with each other and in which respective processing elements of respective second processing units of respective processing subsystems of the **fourth** block are interconnected with each other;

respectively interconnecting respective communication and processing units of the **first** first block of processing subsystems with respective processing elements of a **first** processing unit of a **first** communication and processing subsystem;

respectively interconnecting respective communication and processing units of the **second** block of processing subsystems with respective processing elements of a **second** processing unit of a **first** communication and processing subsystem;

respectively interconnecting respective communication and processing units of the **third** block of processing subsystems with respective processing elements of a **first** processing unit of a **second** communication and processing subsystem;

respectively interconnecting respective communication and processing units of the **fourth** block of processing subsystems with respective processing elements of a **second** processing unit of a **second** communication and processing subsystem;

respectively interconnecting respective communication and processing units of the **first** block of processing subsystems with respective processing elements of a **first** processing unit of a **third** communication and processing subsystem;

respectively interconnecting respective communication and processing units of the **fourth** block of processing subsystems with respective processing elements of a **second** processing unit of a **third** communication and processing subsystem;

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respectively interconnecting respective communication and processing units of the **second** block of processing subsystems with respective processing elements of a **first** processing unit of a **fourth** communication and processing subsystem; and

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respectively interconnecting respective communication and processing units of the **third** block of processing subsystems with respective processing elements of a **second** processing unit of a **fourth** communication and processing subsystem.

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